Amendments to the Specification

Please amend the paragraphs beginning on 18 and continuing to the bottom of page 32 as follows:

Now, the process of the present invention will be described in detail. Referring now specifically to Fig. 3a, this figure refers to power and ground architecture. There is shown in Fig. 3a a silicon substrate 40 over which an interconnect network is created according to the invention, with a wide and thick wire interconnect network created in a thick layer of dielectric overlying a layer of passivation. A power and/or ground pad can be provided for external connection. Following are the various features that are shown in Fig. 3a:

- 40 is the silicon substrate on the surface of which interconnect lines are created in accordance with the invention.
- 42 are semiconductor circuits that are created in or on the surface of substrate 40. Each semiconductor circuit has several nodes connected to other circuits or power/ground.
- 43 is the power or ground node of the semiconductor circuits 42.
- 44 is an ESD circuit that is provided for the protection of circuits 42.
- 58 ~~are connection pads to~~ is a layer including the semiconductor devices 42 that have been created in or on the surface of substrate 40.
- 60 ~~is a layer of fine line interconnects~~ are one or more dielectric layers that ~~has~~ have been created overlying ~~connection pads~~ the layer 58 ~~to~~ including the semiconductor devices 42.

- 61 is a connection comprising metal formed through a via through one or more dielectric layers 60; more such vias are shown in Fig. 3a but are, for reasons of simplicity, not highlighted.
- 62 is a layer of passivation that has been deposited overlying the layer 60 ~~of fine-line interconnects~~.
- 63 is one of the vias that passes through layer 62 of passivation; more such vias are shown in Fig. 3a but are, for reasons of simplicity, not highlighted.
- 64 is a layer of dielectric in which, as a post-passivation process, interconnects have been created.
- 65 is a power or ground bus that is connected to the ESD circuit 44, originating in layer 64 and further passing through layers 62 and 60. This connection comprises metal formed through vias in the dielectric layers 62 and 60.
- 66 is the ~~combined (for multiple connection scheme in layer 64)~~ power or ground bus for the connection scheme in layer 64. This ~~layer~~ power or ground bus 66 could be one or more than one thick, wide metal layers ~~as well as intervening~~ in dielectric layer 64 including a polymer. For multiple layers of metal, the metals are connected through vias in the polymer.
- 67 is a via that is created overlying the layer 62 of passivation and in the dielectric layer 64; more such vias are shown in Fig. 3a but are, for reasons of simplicity, not highlighted.
- 68 is the power ~~of~~ or ground pad for the multiple semiconductor devices 42 in layer 58.

From the representation that is shown in Fig. 3a, it is clear that, most importantly, the ability to create interconnects to semiconductor devices 42 that have been created in or on the surface of a substrate 40 has been extended by creating these interconnects not only as fine-line

interconnects 61 in layer 60 but extending the interconnect by creation of a wide, thick wire interconnect network 66 overlying a layer of passivation 62. This provides immediate and significant benefits in that these lines are further removed from the surface of the substrate 40 (reducing parasitic influences by the interconnect lines on the semiconductor devices 42 that are created in or on the surface of the substrate 40) while the interconnect network 66 that is created overlying the layer of passivation 62 can now contain sturdier; that is, thicker and wider, interconnect lines. The thick, wide metal interconnects 66 can be used for power and ground distribution; this distribution then takes place above a layer of passivation 62 and partially replaces and extends the conventional method of having for these purposes a fine-line distribution interconnect network under the layer of passivation 62.

Some points of interest can be listed at this time as they relate to prior art methods and to the invention.

Prior Art:

- provides an ESD circuit for each pad that is used for external input/output interconnect
- provides~~, after ESD stimuli have passed through the ESD circuits,~~ a fine-line interconnect network for further distribution of the power and ground stimuli, and
- the fine-line power and ground distribution network is created underneath a layer of passivation.

In this respect and related to the above provided comments, it must be remembered that power and ground pads do not require drivers and/or receiver circuitry.

The invention:

- does not need to create an ESD circuit for each pad that is used for external input/output interconnect~~;~~, ~~this~~ in view of the more robust wiring that ~~drives~~ is connected to the ESD circuit, resulting in reduced power loss ~~by an unexpected power surge over the interconnect line,~~ and resulting in more power being delivered to the ESD circuit, and
- allows for the power and ground interconnects to be directly connected to the power and ground nodes of the internal circuits of a semiconductor device, ~~this~~ either without an ESD circuit or with a smaller than regular ESD circuit (as previously explained).

The method that is used to create the interconnect network that is shown in Fig. 3a addresses only the use of power and ground connections. Fig. 3a can be summarized as follows: a silicon substrate 40 is provided in the surface of which there have been created semiconductor devices 42 and at least one electrostatic discharge (ESD) circuit 44; a one or more layers 60 of dielectric are deposited over the substrate 40; a fine-line interconnect network 61 is created in the dielectric layers 60 making contact with the active circuits 42 and the ESD circuit 44. A layer of passivation 62 is deposited over the fine-line interconnect network 61. Openings are created in the layer 62 of passivation that aligns with points of contact in the top layer of the fine-line interconnect network 61. A thick layer 64 of dielectric is optionally deposited over the layer 62 of passivation; a wide thick line interconnect network 66 is created in the layer 64 of dielectric~~,~~ ~~contacting~~ and connected to the ESD circuits. A point of electrical contact 68 comprising a power or ground contact is provided in the surface of the thick layer 64 of dielectric.

Fig. 3b provides further insight into the creation of the power and ground interconnect lines of the invention whereby these interconnect lines have been shown as interconnect lines 66

and interconnect lines 66'. Interconnect lines 66 have been created above the layer 62 of passivation and act as global power and ground interconnect lines. Interconnect lines 66' have been created below the layer 62 of passivation and act as local power and ground interconnect lines.

Fig. 3c provides an alternative in which contact is made to a conventional aluminum metal 61', for example, through the passivation layer 62 rather than making contact to the post-passivation thick, wide metal system 66. The top layer of metal 61' is used for wirebonding purposes and for connection between wirebonding pads and the wide, thick interconnect lines 66. The distance of 61' is a short distance; for example, < 500 μm in length.

In the process of the present invention, in all aspects shown in the figures, the post passivation metallization 66 can optionally be performed directly on the passivation layer 62 without the intervening polymer layer. Although the polymer layer provides distinct advantages, it may be desirable to dispense with the polymer layer in order to save costs.

Referring now to Fig. 4a, Fig. 4a addresses the interconnections of signal and clock line. Signal here includes address, data, logic, and analog signals. Signal also includes the power/ground voltage output from voltage regulators. In Fig. 4a there is shown a cross section of a silicon substrate 40 over which an interconnect network 61 is created according to the invention. An access pad 70 to an ESD circuit 45 or driver or receiver circuits or I/O circuits 45' is provided through ~~the surface of~~ the layers 64 and 60 of dielectric for external connection. While an ESD circuit 45 is required for all circuits 42 to which an I/O connection is established ~~and independent of the type of circuit to which the I/O connection is established~~, the I/O ~~interconnect~~ connection can also be provided to a receiver circuit or a driver circuit or an I/O circuit 45'.

The features not previously highlighted that are shown in Fig. 4a are:

- the invention provides an interconnect network 72 comprising wide, thick interconnect lines for distribution of the clock and signal stimuli,
- the invention creates an interconnect network 72 of thick, wide interconnect lines for the clock and signal stimuli overlying a layer of passivation 62,
- 70 is an external connection (pad) that is provided for the ESD circuit 45 and for driver/receiver/I/O circuit 45'; pad 70 provides external access for clock and signal stimuli to circuits 45 and 45', and
- 72 is a clock or signal bus that is created in the ~~interconnect~~ dielectric layer 64 using thick, wide wires for interconnect lines; it must be noted that the clock and signal interconnect line distribution 72 is entirely contained within the layer 64 without providing an external point of I/O interconnect.

The method that is used to create the interconnect network that is shown in cross section in Fig. 4a can be summarized as follows. A silicon substrate 40 is provided; active circuits have been created in the surface of the substrate 40 including an ESD circuit 45 and the~~,~~ receiver, driver and I/O circuit 45'. First layers 60 of dielectric of inorganic material are deposited over the substrate 40 and a fine-line interconnect network 61 is created in the layers 60 of dielectric, making contact with the active circuitry 45, 45', and 42. A layer 62 of passivation is deposited over the first thin layers 60 of dielectric; a pattern 63 of metal plugs is created in the layer 62 of passivation (or, for low aspect ratio openings, direct contact is established between overlying layers 72 of metal through an opening in an interposed layer 64 of dielectric); the metal interconnects 67 align with points of electrical contact in the surface of the first layers 60 of

dielectric. One or more thicker layers 64 of dielectric are deposited over the surface of the layer 62 of passivation, typically of an organic material; a wide thick line interconnect network 72 is created in the thicker layer 64 of dielectric, making electrical contact with the metal plugs or the metal pads in or under the layer 62 of passivation~~, including to the one ESD,~~ connected to the receiver, driver or I/O circuit 45'. A point of electrical contact 70 is provided in the surface of the second layer 64 of dielectric and connected to the ESD~~,~~ circuit 45 and the receiver, driver or I/O circuit 45'.

Fig. 4b provides further insight into the creation of the signal and clock interconnect lines of the invention whereby these interconnect lines have been shown as interconnect lines 71 and interconnect lines 71'. Interconnect lines 71 have been created above the layer 62 of passivation and act as global signal and clock interconnect lines. Interconnect lines 71' have been created below the layer 62 of passivation and act as local signal and clock interconnect lines. Furthermore, internal circuits 42 have no driver, no receiver, and no ESD connections.

Intra-chip drivers and receivers 80 may be necessary if the interconnection distance is long and/or the load of the net of circuits 42 is large, as shown in Figs. 4c and 4d. A driver circuit is used to drive a load; i.e., to drive current. A driver current is the output of a driver circuit. The ability to drive current is proportional, in CMOS devices, to the W/L ratio, where W/L is the ratio of the device channel width to its length. These intra-chip drivers 80 are typically smaller than I/O drivers 45'. ~~Intra-chip drivers and receivers 80 are shown in Figs. 4c and 4d.~~ Intra-chip circuits 80 typically have no ESD circuits and no I/O circuits. For short distance on-chip interconnection, no intra-chip circuits may be required. Fig. 4c shows an interconnecting structure 72 connecting multiple intra-chip drivers or receivers 80, which are connected in series to the internal circuits 42. Fig. 4d shows an example of internal circuits 42 that need to utilize attached intra-chip drivers or receivers while internal circuits 42' do not

require attached intra-chip drivers or receivers. Also shown in Fig. 4d is an interconnecting structure 71 connecting multiple intra-chip drivers or receivers 80, which are connected in series to the internal circuits 42.

Further provided are:

- 45 are two ESD circuits that are provided in or on the surface of the substrate 40, as shown in Figs. 4a-4d; ESD circuits are always required for any external connection to an input/output (I/O) pad
- 45' which are circuits that can be receiver or driver or I/O circuits for input (receiver) or output (driver) or I/O purposes respectively, as shown in Figs. 4a-4d. These are off-chip drivers or receivers or I/O circuits.

Intra-chip circuits 80 are usually smaller than the off-chip drivers 45'. The intra-chip driver circuits 80 are different from the off-chip circuits 45' in that they have no I/O circuits and no ESD circuits. Figs. 4c and 4d show smaller internal driver circuits 80 connected to the internal circuits 42. 45' are larger off-chip circuits.

Fig. 5a shows a representation of a silicon substrate 40 over which an interconnect network 74 is created according to the invention, with the interconnect network 74 created in a thick layer 64 of dielectric overlying a layer 62 of passivation ~~and remaining internal to the thick layer of dielectric~~. No ESD circuit, receiver, driver or I/O circuit access pad is provided for external connection to the internal circuits 42. Shown in Fig. 5a and not previously highlighted is the clock or signal interconnect line 74, providing for an interconnect scheme of thick, wide lines overlying a passivation layer 62 whereby no external I/O connections are provided. Due to the

thick, wide lines of the interconnect network 74 that is created overlying a passivation layer 62, the clock and signal distribution can take place entirely within the ~~interconnect~~ dielectric layer 64; this as opposed to prior art methods where, for clock and signal distribution lines, each thick, wide interconnect line (where such thick, wide interconnect lines are used) must be provided with at least one I/O connect point for off-chip connection.

The method that is used to create the wide thick line interconnect lines 74 that is shown in cross section in Fig. 5a can be summarized as follows and is similar to that described above for Fig. 4a. A silicon substrate 40 is provided~~,~~. ~~a~~Active devices have been provided in the surface of the substrate. First thin layers 60 of dielectric are deposited over the surface of the substrate 40, a fine-line interconnect network 61 is created in the first layers 60 of dielectric, comprising fine-line interconnect lines, making contact with points of electrical contact in the surface of the substrate 40. A layer of passivation 62 is deposited over the surface of the first layers 60 of dielectric, a pattern of conductive interconnects 63 is created in the layer 62 of passivation ~~that~~ and aligns with the points of electrical contact in the surface of the first layer 60 of dielectric. One or more second layers 65 of dielectric are deposited over the surface of the layer 62 of passivation, the interconnecting structure 74 making electrical contact with the conductive interconnects 63 in the layer 62 of passivation. Fig. 5a shows a series of driver/receivers, or transceivers, or repeater devices 101 and 102. Receivers 101 are connected to drivers 102.

Fig. 5b provides further insight into the creation of the signal and clock interconnect lines of the invention whereby these interconnect lines have been shown as interconnect lines 71 and interconnect lines 71'. Interconnect lines 71 have been created above the layer 62 of passivation and can act as global signal and clock interconnect lines. Interconnect lines 71' have been created below the layer 62 of passivation and act as local signal and clock interconnect lines. Also as shown in Fig. ~~5a~~5b, internal circuits 42 are shown. Circuits 42 have no I/O circuits and

no ESD circuits. Figs. 5c and 5d show smaller internal driver circuits 80 connected to the internal circuits 42. Figs. 5c and 5d show an interconnecting structure 74 connects multiple intra-chip drivers or receivers 80, which are connected in series to the internal circuits 42.

It must further be emphasized that, where Figs. 3-5 show a fine-line interconnect network ~~60~~ 61 that underlies the layer 62 of passivation, the invention also enables and can be further extended with the complete elimination of the fine-line interconnect network ~~60~~ 61 and creating an interconnect network in the dielectric layer 64 that uses only thick, wide wires. For this application of the invention, the first layer of dielectric 60 is not applied, the layer 62 of passivation is deposited directly over the surface of the created semiconductor devices 58 in or on the surface of substrate 40.

It is further of value to briefly discuss the above implemented and addressed distinction between fine-line interconnect lines and wide, thick interconnect lines. The following points apply in this respect:

- the prior art fine line interconnect lines are created underneath a layer of passivation, the wide, thick interconnect lines of the invention are created above a layer of passivation
- the fine-line interconnect lines are typically created in a layer of inorganic dielectric, the thick wide interconnect lines are typically created in a layer of dielectric comprising polymer. This is because an inorganic material cannot be deposited as a thick layer of dielectric because such a layer of dielectric could develop fissures and crack as a result. Although the polymer is preferred, the thick wide interconnect lines could be formed over a conventional passivation layer without the polymer.

- fine-line interconnect metal is typically created using methods of sputter with resist etching or of damascene processes using oxide etch with electroplating after which CMP is applied. Either one of these two approaches cannot create thick metal due to cost considerations or oxide cracking
- thick, wide interconnect lines can be created by first sputtering a thin metal base layer, coating and patterning a thick layer of photoresist, applying a thick layer of metal by electroplating, removing the patterned photoresist and performing metal base etching (of the sputtered thin metal base). This method allows for the creation of a pattern of very thick metal; metal thickness in excess of 1 μm can in this manner be achieved while the thickness of the layer of dielectric in which the thick metal interconnect lines are created can be in excess of 2 μm.